Interconnection Networks

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- Butterfly
- Cube connected Cycle
- Tree and Xtree
- Shuffle exchange
- CrossBar
- Multi Stage

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Butterfly Network

•A butterfly network consists of **(K+1)2^k** nodes divided into **K+1** Rows, or Ranks.

• Let node (i,j) refer to the j_{th} node in the i_{th} Rank. Then for i>0 node (i,j) is connected to 2 nodes in Rank i-1, node (i-1,j) and node (i-1,M), where M is the integer found by inverting the i_{th} most significant bit of j.

• Note that if node (I,j) is connected to node (i-1,M), then node (1,M) is connected to node (i-1,j). This forms a butterfly pattern.

❑ Network diameter=2K
❑ Bisection Width=2^K

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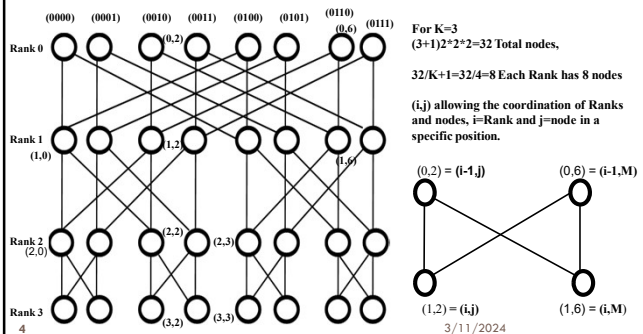

For K=3
(3+1)2*2*2=32 Total nodes,

32/K+1=32/4=8 Each Rank has 8 nodes

(i,j) allowing the coordination of Ranks and nodes, i=Rank and j=node in a specific position.

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Cube Connected Cycles

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- CCC is an unidirected graph, formed by replacing each vertex of a hypercube graph by a cycle
- CCC of order n (denoted CCCn) can be defined as a graph formed from a set of $n2^n$ nodes, indexed by pairs of numbers (x, y) where $0 \le x < 2^n$ and $0 \le y < n$
- Each such node is connected to three neighbors: (x, (y + 1) mod n), (x, (y − 1) mod n), and (x ⊕ 2y, y), where "⊕" denotes the bitwise exclusive or operation on binary numbers

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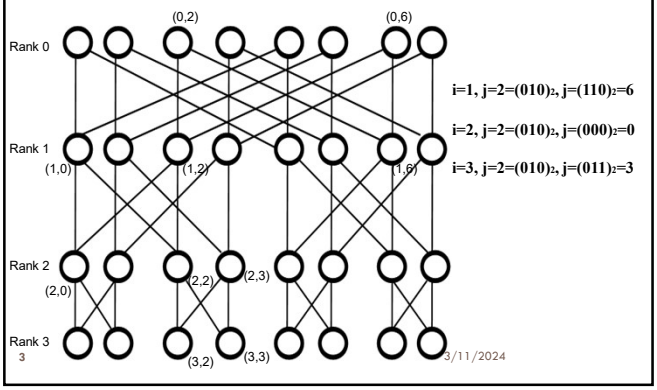
Example of a Butterfly Network

Here is a Butterfly Network for **K=3**



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Cube Connected Cycles Cont.

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- An n-cube network has n2n nodes where two nodes are connected if the binary representation of their addresses differs by one and only one bit
- Each node can be identified by a pair (x, y) of integers, where x is the cycle number (the node number in the original hypercube) and y is the node number within the cycle
- This same numbering scheme is applicable to the representation below

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Transformation of a Hypercube to CCC

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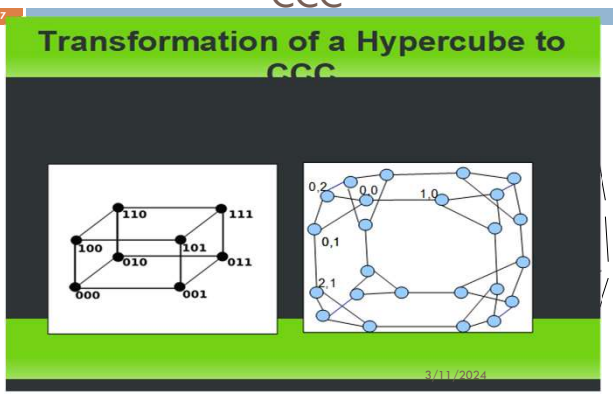

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Tree Topology

- Nodes at one level can only connect to nodes in adjacent levels
- A node may have only one parent even though it may give rise to several children.
- Nodes that do not have any children are called 'terminal nodes'
- The Figures below illustrates both the binary and ternary trees.

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CCC

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- Advantage
  - The advantage of cube-connected cycles is that the node's degree is always 3, independent of the value of n
- Disadvantage of CCC
  - CCC tends to suffer from considerable performance degradation when fault arises

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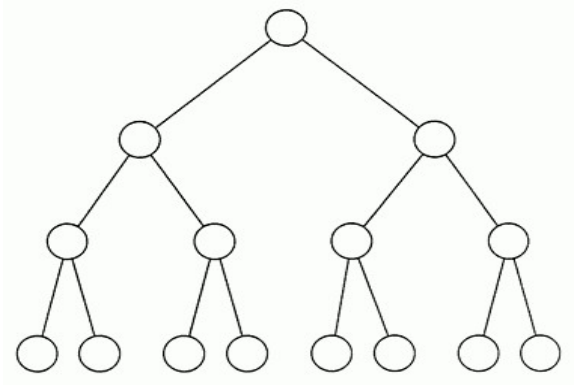
Binary Tree



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Tree Topology

'Trees topologies' are hierarchical structures that have some resemblance to natural trees.

- Its starts with a node at the top called the root.
- This node is connected to other nodes by 'edges' or 'branches'.
- The nodes may spawn further nodes forming a multilayered structure.

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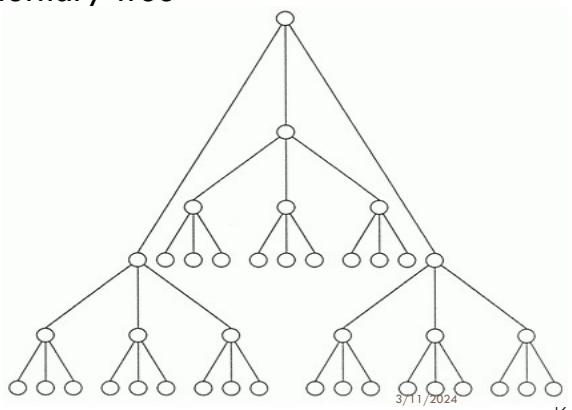
Ternary Tree



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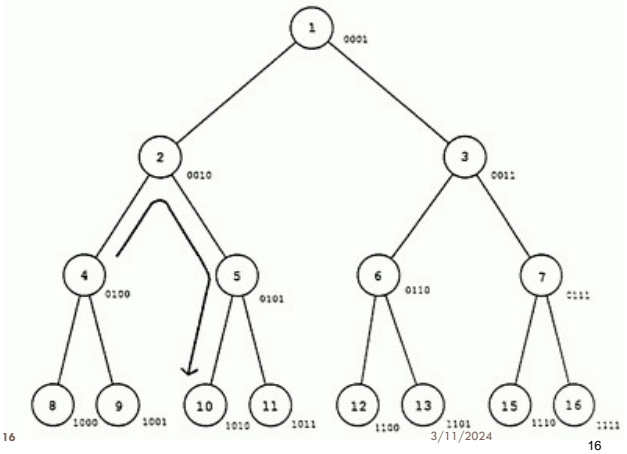
Tree Topology

- By examining the figures it can be seen that there is only one path between any two nodes.
- A message from one terminal node to another terminal node has to be routed back up the tree to the first node that is common to both the sender and the receiver.
- Once the message arrives at the common parent it can then travel back down the tree to the receiving node.



Tree Topology

- An important step in finding the message path involves finding the first node that is common to both sender and receiver
- This can be done by generating two lists of successive parents all the way up to the root.
- One list for the sender and one for the receiver
- The parent of the current node can be found by dividing the address by two and taking the modulus

Message Passed from Node 4 to Node 10 in a Binary Tree

Path from Node to Root

Sender		Receiver	
Binary	**Decimal**	**Binary**	**Decimal**
0100	4	1010	10
0010	2	0101	5
0001	1 (root)	0010	2
		0001	1 (root)

Tree Topology

- Path finding can be illustrated with reference to figure 3.
- Let node four be the sender and node ten the receiver.
- The list of successive parents will be as follows:

X-Tree Topology

- It can be seen that the first node to appear in both lists is 2.
- The path is generated by traversing down the sender list as far as the common node (in this case 2),
- and then up the receiver list from the common node to the top.
- A disadvantage of this topology is that there is no alternative route if a necessary link fails.

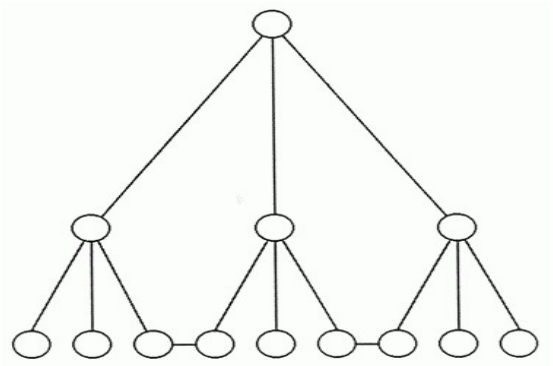
X-Tree Topology

- One way to alleviate this communication problem is to add links between branches at the same level.
- The resulting structure is called an 'X-tree' .
- X-tree is an extended tree topology as shown in figure 4 below:

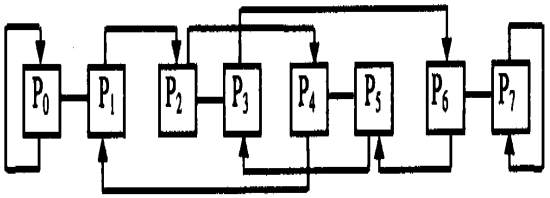
SHUFFLE EXCHANGE

•Consider a set of N processors, numbered P_0, P_1, … P_{N-1}
•Perfect shuffle connects processors P_i and P_j by a one-way communications link,
•If j = 2*i for 0 <= i <= N/2 – 1 or j = 2*i + 1 – N otherwise.
•See below an example for N= 8 where arrows represent shuffle links and solid lines represent exchange links.

An X-Tree topology



SHUFFLE EXCHANGE



X-Tree Topology

- Like the ring, it uses direct connections between processors; each having three connections.
- There is only one unique path between any pair of processors.
- The X-tree therefore avoids overlap whenever it is possible without allowing the tree to degenerate.
- Therefore the Extended-tree (X-tree) topology provides availability of communication between nodes if one link fails.

SHUFFLE EXCHANGE

- In other words, perfect shuffle connects processor I with (2*I modulo (N-1)), with the exception of the processor N – 1 which is connected to itself.
- Having trouble with this logic
- Consider the following:

SHUFFLE EXCHANGE

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- Let's represent numbers i and j in binary.
- If j can be obtained from i by a circular shift to the left, then P_i and P_j are connected by one-way communications link, viz.:

Architecture

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- A crossbar switched network is a single stage network built with unary (single) switches at the cross point.
- At each intersection is a **cross point** - a switch that can be opened or closed
- It is an assembly of switches (switching nodes) between multiple inputs and multiple outputs arranged in the form of a matrix.
- If a crossbar has 'n' inputs and 'n' outputs, then it has a matrix with n*n cross points.
- At each cross point is a switch, when closed connects one of the 'n' inputs to one of 'n' outputs.

SHUFFLE EXCHANGE

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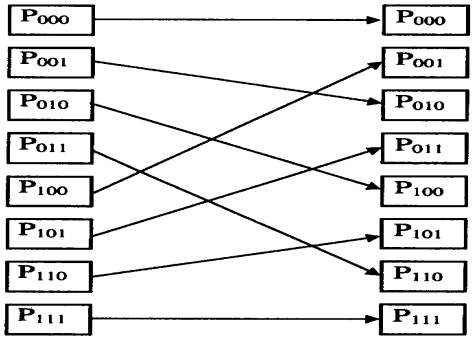

Architecture

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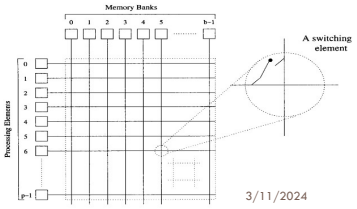
- It is a non-blocking network that allows a multiple input/ output connection pattern to be achieved simultaneously.
- The cross bar switch provides all possible permutations



Crossbar Interconnection

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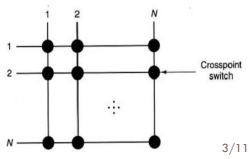
A dynamic switch-based network, where all processors have dedicated buses directly connected to all memory blocks and can provide simultaneous connections among all its inputs and all its outputs.



Crossbar Interconnection

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- Example: sending a message from input 6 to output 5:
- Source-> switchbox (6,1)->(6,2).....(6,5)

  ->(4,5)->(3,5).....-> destination.
  - A processor can access a particular memory block as long as it has highest priority to that memory block. If some other processor gets highest priority for that particular memory block, the processor, which is currently accessing the memory block gets its connection disconnected. It will have to wait until it gets the highest priority for accessing that block again.

Crossbar Interconnection

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- Some factors to be considered with regards to a Crossbar:
- **Scalability**: This refers to the change in performance by increasing or decreasing the number of memory modules.
- **Reliability**: This refers to the impact on the system when a switch, wire, or any other part of the network breaks down.
- **Latency**: It refers to the time required by the processor to access memory

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Advantages of Cross-bar Switch networks

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- Every node is connected to all others (non-blocking).
- It provides full connectivity.
- Low latency and high throughput
- Highly useful in multiprocessor systems , as all processors can send memory requests independently and asynchronously.
- Potential for speed: in one clock a connection can be made between a source and destination.

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Disadvantages of Cross-bar Switch networks

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- Complexity increases with an increase in number of inputs (processors) or number of outputs (memory)
- Too expensive for a large of number of processors.

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Multi Stage Interconnection Networks

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- A network formed by interconnecting a set of nodes through a switching fabric.
- Nodes can either be programmable computers or memory blocks.
- Switching fabric consists of a set of switches interconnected to form a topology with defined connection points for the nodes.

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Multi Stage Interconnection Networks

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- Switches are organized in stages, thus the name multistage
- A MIN normally connects N input to N outputs and is referred to as N x N MIN.
- The parameter N is called the size of the network.

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Multi Stage Interconnection Networks

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- multistage interconnection networks as: are a class of high-speed computer networks usually composed of processing elements (PEs) on one end of the network and memory elements (MEs) on the other end, connected by switching elements (SEs).
- The switching elements themselves are usually connected to each other in stages, hence the name.

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DIFFERENCE BETWEEN SINGLE STAGE AND MULTI-STAGE INTERCONNECTION

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- In single stage networks data may have to pass through the switching elements several times before reaching the final destination.
- In Multistage one pass is sufficient for data to traverse from input to output.

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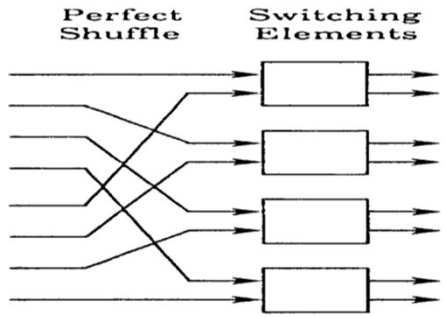

CONSTRUCTION

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- If we cascade(arrange in a series or sequence) single staged networks together, they form a completely connected multistage interconnection network and data is no longer required to circulate the network but instead is sent from input side to output side.

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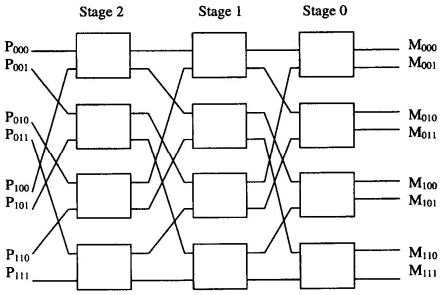

HOW ARE MINs CONSTRUCTED?

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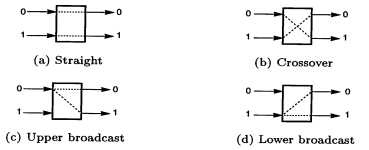
- By using smaller switches, usually 2x2,connected by fixed links
- These 2x2 switches have two possible settings for permutation networks, straight and exchange, as shown in the figure below:



HOW ARE MINS CONSTRUCTED

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- Inputs and outputs are connected in a 1 to 1 manner.
- The source node generates a tag, which is binary equivalent of the destination.
- At each switch, the corresponding tag bit is checked.
- If the bit is 0, the input is connected to the upper output.
- If it is 1, the Input is connected to the lower output.

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- MINs networks can be classified into the following 2 categories:

Non-blocking Networks	• A network is called strictly non-blocking if it can connect any idle input to any idle output regardless of what other connections are currently in process.
Re-Arrangeable Non-Blocking Networks	• In this case a network should be able to establish all possible connections between inputs and outputs by rearranging its existing connections.
Blocking Networks	• A network is said to be blocking if it can perform many, but not all, possible connections between terminals.

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ADVANTAGES OF MINS

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- Multistage interconnection networks (MINs) are used in multiprocessing systems to provide cost-effective, high bandwidth communication between processors and/or memory modules.
- Multistage interconnection networks attempt to reduce cost and decrease the path length.

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DISADVANTAGES

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- The most obvious problem of MINs is the blocking problem and impossibility of the implementation of appropriate routing algorithms since there is only a unique path between every input-output pair.
- The switch box is the basic component of the network, the cost of the network (in hardware terms) is measured by the number of switch boxes required.

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